IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please AMEND the title of the invention in accordance with the following:

PROCESSING APPARATUS AND INTEGRATED CIRCUIT TO PREVENT ILLICIT ACCESS AND REVERSE ENGINEERING

IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Page 19, paragraph beginning at line 23

The address decoder 104 inputs the address A1 and receives the area information indicating to-be-ciphered areas from the ciphering information register 103. Then, the address decoder 104 outputs chip select signals CS0 to ~~SC6~~ CS6 to an access target device and outputs a ciphering control signal Crp indicating which device is an access target and whether or not it is necessary to conduct ciphering, to the ciphering circuit 121.

Page 39, paragraph beginning at line 16

Fig. 17 is ~~s~~ a flow chart showing a flash ROM scrambling part of the program operating when the apparatus is powered after a state in which the flash ROM is scrambled before shipment from the factory, a scramble pattern for descrambling the scrambled flash ROM is ciphered by a public key Kpb and stored in the backup RAM.